What is claimed is:

1. A speed converter for converting the speed of packets transmitted between first and second communication nodes respectively attached to first and second IEEE-1394 serial buses, comprising:

a first transceiver node for receiving an inbound first packet at a first speed from the first bus and transmitting an inbound second packet as an outbound second packet at the first speed to the first bus;

a second transceiver node for transmitting said inbound first packet as an outbound first packet at a second speed to the second bus and receiving said inbound second packet at the second speed from the second bus; and

header translation circuitry for translating destination identifier of said inbound first packet to destination identifier of said outbound first packet according to a mapped relationship between the first transceiver node and the second communication node, and translating destination identifier of said inbound second packet to destination identifier of said outbound second packet.

2. The speed converter of claim 1, wherein the first transceiver node comprises:

a first physical layer processor connected to said first bus;

a first link layer processor connected to the first physical layer processor; and

first speed setting means for setting a value representative of said first speed into said first link layer processor,

wherein said second transceiver node comprises:

a second physical layer processor connected to said second bus;

a second link layer processor connected to the second physical layer processor; and

second speed setting means for setting a value representative of said second speed into said second link layer processor,

wherein said header translation circuitry comprises:

a memory for storing identifiers for mapping said first transceiver node to said second communication node; and

control circuitry connected to said first and second link layer processors for receiving a packet therefrom and rewriting destination identifier of the packet according to the identifiers stored in said memory when a transaction is initiated from said first bus.

3. The speed converter of claim 1, wherein said memory further stores identifiers for mapping said second transceiver node to said first communication node, and wherein said control circuitry receives a packet from said second transceiver node and rewrites destination identifier of the packet according to the identifiers stored in said memory when a transaction is initiated from said second bus.

4. A speed converter for converting the speed of packets transmitted between a plurality of first communication nodes attached to a first IEEE-1394 serial bus and a plurality of second communication nodes attached to a second IEEE-1394 serial bus, comprising:

at least one first repeater node connected to the first bus;

a first transceiver node for receiving an inbound first asynchronous packet from the first bus at a first speed via said at least one first

repeater node and transmitting an inbound second asynchronous packet as an outbound second asynchronous packet at the first speed to the first bus via said at least one first repeater node, the first transceiver node having identifiers identifying the first transceiver node itself and said at least one first repeater node;

at least one second repeater node connected to the second bus;

a second transceiver node for transmitting said inbound first asynchronous packet as an outbound first asynchronous packet to the second bus at a second speed via at least one second repeater node and receiving the inbound second asynchronous packet from the second bus at the second speed via said at least one second repeater node and receiving said inbound second asynchronous packet at the second speed from the second bus via said at least one second repeater node, the second transceiver node having identifiers identifying the second transceiver node itself and said at least one second repeater node; and

header translation circuitry for translating destination identifier of said inbound first asynchronous packet received by the first transceiver node to destination identifier of said outbound first asynchronous packet according to mapped relationships between said second communication nodes and said first transceiver node and said at least one first repeater node, and translating destination identifier of said inbound second asynchronous packet received by the second transceiver node to destination identifier of said outbound second asynchronous packet according to mapped relationships between said first communication nodes and said second transceiver node and said at least one second repeater node.

5. The speed converter of claim 1 or 4, wherein said second transceiver node receives, from the second bus, an isochronous packet containing a first channel number at said second speed, and wherein said first transceiver node receives the isochronous packet from the second transceiver node and translates the first channel number of the received packet to a second channel number and transmits the isochronous packet containing the second channel number at said first speed to the first bus.

6. The speed converter of claim 1 or 4, further comprising means for synchronizing clock timing of said first transceiver node to clock timing of said second transceiver node.

7. The speed converter of claim 4, wherein the first transceiver node comprises:

a first physical layer processor;

a first link layer processor connected to the first physical layer processor; and

first speed setting means for setting a value representative of said first speed into said first link layer processor,

wherein said at least one first repeater node comprises a third physical layer processor connected in series between said first bus and said first physical processor;

wherein said second transceiver node comprises:

a fourth physical layer processor;

a second link layer processor connected to the fourth physical layer processor; and

second speed setting means for setting a value representative of said second speed into said second link layer processor,

wherein said at least one second repeater node comprises a fifth physical layer processor connected in series between said second bus and said fourth physical processor;

wherein said header translation circuitry comprises:

a memory for storing identifiers for mapping said second communication nodes to said first transceiver node and said at least one first repeater node and storing identifiers for mapping said first communication nodes to the second transceiver node and said at least one second repeater node; and

control circuitry connected to said first and second link layer processors for receiving an asynchronous packet therefrom and rewriting destination identifier of the asynchronous packet according to the identifiers stored in said memory when a transaction is initiated from each of said first and second buses.

8. The speed converter of claim 2 or 7, wherein said first link layer processor includes first register means for setting a first channel number and said second link layer processor includes second register means for setting a second channel number,

said second link layer processor receiving an isochronous packet containing said second channel number from said second bus at said second speed and forwarding the received packet to said first link layer processor via a data path,

said first link layer processor translating the channel number of said isochronous packet forwarded from said second link layer

processor to said first channel number and transmitting the channel number translated isochronous packet toward the first bus at said first speed.

9. The speed converter of claim 4,

wherein the first transceiver node is responsive to receipt of a first asynchronous request packet requesting start or end of transmission of isochronous packets from said first bus for forwarding the received first asynchronous request packet to said second transceiver node,

wherein the second transceiver node is responsive to the first asynchronous request packet from the first transceiver node for setting the second transceiver node in a state for preparing start or end of transmission of isochronous packets to said second bus,

wherein the first transceiver node is responsive to receipt of a second asynchronous request packet requesting start or end of reception of isochronous packets from said first bus for setting the first transceiver node in a state for preparing start or end of transmission of isochronous packets to the first bus.

10. The speed converter of claim 9,

wherein the second transceiver node transmits an asynchronous request packet to the second bus requesting one of the communication nodes on the second bus for starting or ending transmission of isochronous packets when the first transceiver node receives said first asynchronous request packet from the first bus,

wherein the second transceiver node transmits an asynchronous request packet to the second bus requesting said one communication

node to set in a state preparing for start or end of reception of isochronous packets when the first transceiver node receives said second asynchronous request packet from the first bus.

11. The speed converter of claim 10, wherein one of said first and second transceiver nodes includes bus reset recovery means responsive to an occurrence of a bus reset for resetting said one of the communication nodes in the state which was attained when said bus reset occurred.

12. The speed converter of claim 10, wherein said first transceiver node includes an output master plug register (oMPR), an input master plug register (iMPR), an output plug control register (oPCR) and an input plug control register (iPCR), all of said plug and control registers being specified according to IEC-61883 standard,

wherein said first transceiver node (211) is arranged to initialize said plug and control registers according to values set in said one communication node on said second bus, and modify values set in data rate capability field of said oMPR and iMPR and a value set in data rate field of said oPCR to said first speed.

13. The speed converter of claim 12,

wherein said first transceiver node translates a first channel number contained in a first isochronous packet from said second bus to a second channel number set in channel number field of said oPCR when a value indicating transmission of an isochronous packet is set in said oMPR,

wherein said first transceiver node translates the second channel number contained in a second isochronous packet from said first bus to said first channel number contained in said first isochronous packet when a value indicating reception of an isochronous packet is set in said iPCR.

14. The speed converter of claim 13, wherein said first channel number is a default number of decimal 63.

15. The speed converter of any one of claims 4 to 14, wherein the asynchronous packet received from one of said first and second buses is a configuration ROM read request packet for accessing a configuration ROM having a bus address in the range between a hexadecimal value of FFFF F000 0400 and a hexadecimal value of FFFF F000 07FC.

16. The speed converter of any one of claims 4 to 14,

wherein said memory stores configuration ROM data of the communication nodes of said first and second buses,

wherein said first transceiver node is responsive to receipt of a configuration ROM read request packet from said first bus for reading configuration ROM data from said memory corresponding to the destination identifier contained in the received read request packet and transmitting a read response packet to the first bus containing the read configuration ROM data,

wherein said second transceiver node is responsive to receipt of a configuration ROM read request packet from said second bus for reading configuration ROM data from said memory corresponding to

the destination identifier contained in the received read request packet and transmitting a read response packet to the second bus containing the read configuration ROM data.

17. The speed converter of claim 16, wherein the configuration ROM data stored in said memory by rewriting lower 64 bits of Bus_Info_Block of configuration ROM data of each of said communication nodes and lower 64 bits of Node_Unique_Id leaf with 64-bit Extended Unique Identifier and rewriting module_vendor_id field of Module_Vendor_Id entry with a company ID indicating the manufacturer of the speed converter.

18. A speed converter for converting the speed of packets transmitted between a plurality of first communication nodes attached respectively to a plurality of first IEEE-1394 serial buses and at least one second communication node attached to a second bus, comprising:

a plurality of speed conversion units associated respectively with said plurality of first buses, each of said speed conversion units including:

a first transceiver node for receiving an inbound first packet at a first speed from the associated first bus and transmitting an inbound second packet as an outbound second packet at the first speed to the associated first bus;

a second transceiver node for transmitting said inbound first packet as an outbound first packet at a second speed to the second bus and receiving said inbound second packet at the second speed from the second bus; and

header translation circuitry for translating destination identifier of said inbound first packet to destination identifier of said outbound first packet according to mapped relationship between the first communication node of the associated first bus and said at least one second communication node, and translating destination identifier of said inbound second packet to destination identifier of said outbound second packet.

19. A method of converting the transmission speed of packets transmitted between a first communication node and a second communication node respectively attached to first and second IEEE-1394 serial buses, comprising:

receiving, at a first transceiver node, an inbound first packet transmitted at a first speed from said first bus;

translating destination identifier of said inbound first packet to destination identifier of an outbound first packet;

transmitting the outbound first packet from a second transceiver node to the second bus at a second speed;

receiving, at said second transceiver node, an inbound second packet at said second speed from said second bus;

translating destination identifier of said inbound second packet to destination identifier of an outbound second packet; and

transmitting the outbound second packet from the first transceiver node to said first bus at said first speed.

20. The method of claim 19, further comprising:

setting a first channel number in said first transceiver node and setting a second channel number in said second transceiver node;

receiving, at said second transceiver node, an isochronous packet containing a second channel number from said second bus at said second speed;

translating the channel number of said isochronous packet to said first channel number at said first transceiver node; and

transmitting the channel-translated isochronous packet from the first transceiver node to the first bus at said first speed.

21. A method of converting the speed of packets transmitted between a plurality of first communication nodes attached to a first IEEE-1394 serial bus and a plurality of second communication nodes attached to a second IEEE-1394 serial bus, comprising:

receiving, at a first transceiver node, an inbound first packet from the first bus at a first speed via at least one first repeater node;

translating destination identifier of said inbound first packet to destination identifier of an outbound first packet according to relationships between said second communication nodes and said first transceiver node and said at least one first repeater node;

transmitting from a second transceiver node said outbound first packet to the second bus at a second speed via at least one second repeater node;

receiving, at said second transceiver node, an inbound second packet from the second bus at the second speed via said at least one second repeater node;

translating destination identifier of said inbound second packet to destination identifier of an outbound second packet according to relationships between said first communication nodes and said second transceiver node and said at least one second repeater node; and

transmitting from the first transceiver node said outbound second packet to the first bus via said at least one first repeater node at said first speed.

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